

**N-CHANNEL MOS FIELD EFFECT TRANSISTOR
FOR SWITCHING**

DESCRIPTION

The μPA1857 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

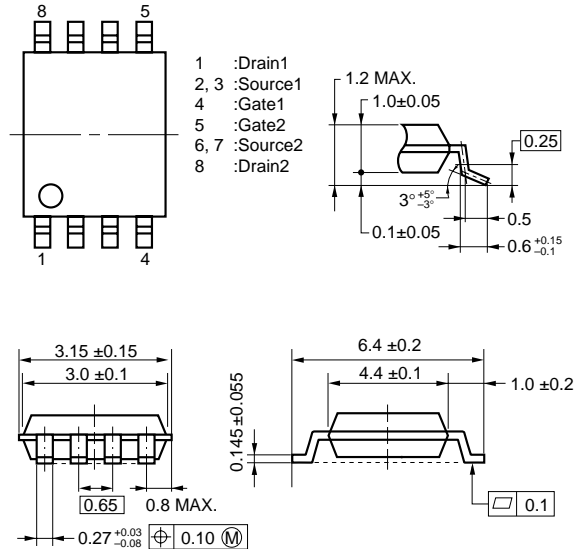
FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 67.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.0 \text{ A)}$
 $R_{DS(on)2} = 86.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 2.0 \text{ A)}$
 $R_{DS(on)3} = 95.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 2.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 580 \text{ pF TYP.}$
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1857GR-9JG	Power TSSOP8

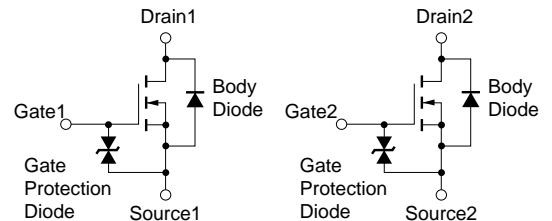
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _A = 25°C)	I _{D(DC)}	±3.8	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±15.2	A
Total Power Dissipation (1unit) ^{Note2}	P _{T1}	1.0	W
Total Power Dissipation (2unit) ^{Note2}	P _{T2}	1.7	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note3}	I _{AS}	3.8	A
Single Avalanche Energy ^{Note3}	E _{AS}	33	mJ

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

2. T_A = 25°C Mounted on ceramic substrate of 50 cm² x 1.1 mm

3. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V, V_{DD} = 30 V

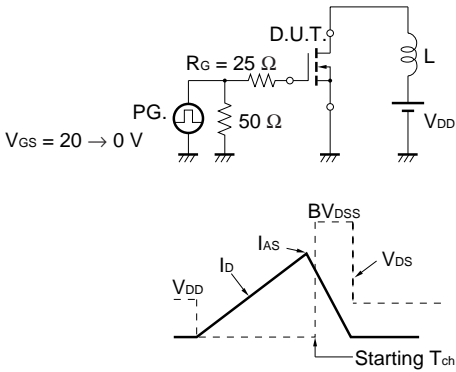
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

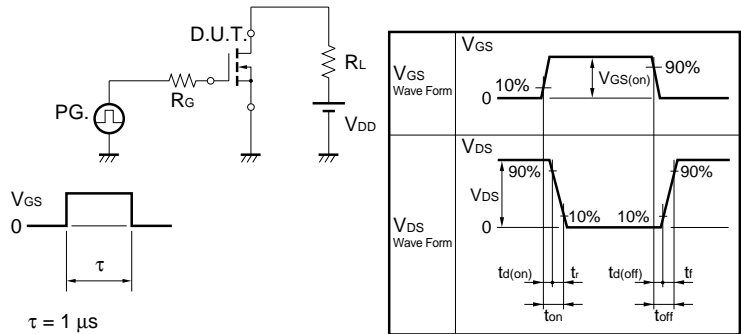
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 2.0 A	2.5	5.4		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 2.0 A		53	67.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 2.0 A		64	86.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 2.0 A		71	95.0	mΩ
Input Capacitance	C _{iSS}	V _{DS} = 10 V		580		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		50		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 2.0 A		10		ns
Rise Time	t _r	V _{GS(on)} = 10 V		9		ns
Turn-off Delay Time	t _{d(off)}	R _G = 6 Ω		32		ns
Fall Time	t _f			4		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		12		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2		nC
Gate to Drain Charge	Q _{GD}	I _D = 3.8 A		3		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 3.8 A, V _{GS} = 0 V		0.80		V
Reverse Recovery Time	t _{rr}	I _F = 3.8 A, V _{GS} = 0 V		33		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		58		nC

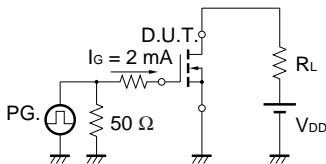
TEST CIRCUIT 1 AVALANCHE CAPABILITY



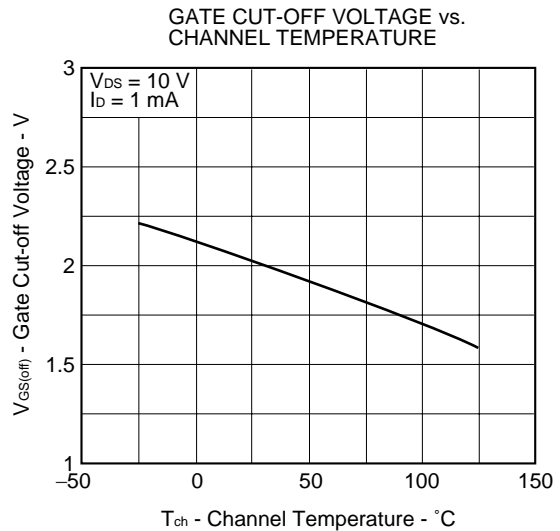
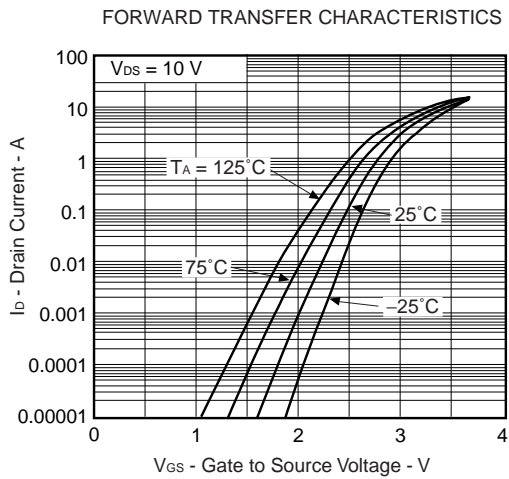
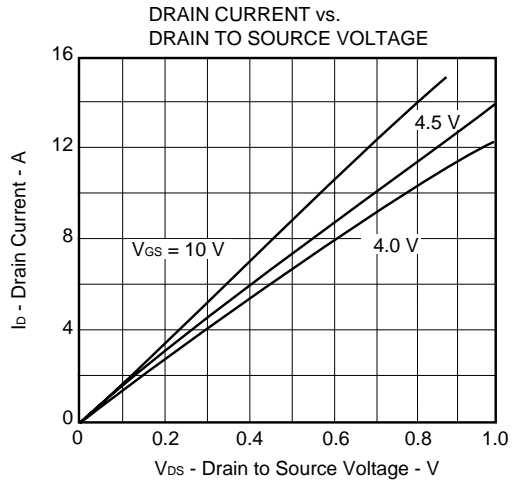
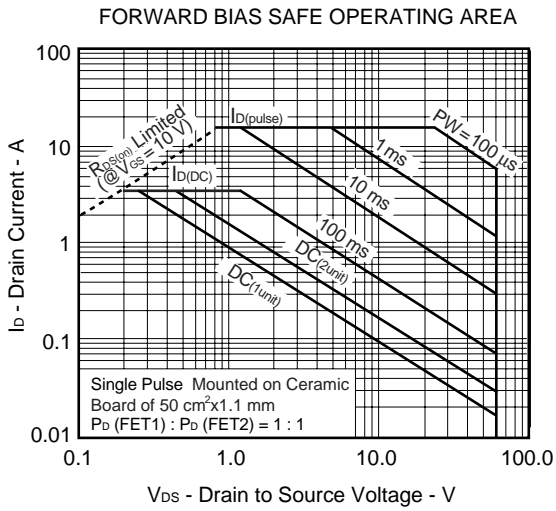
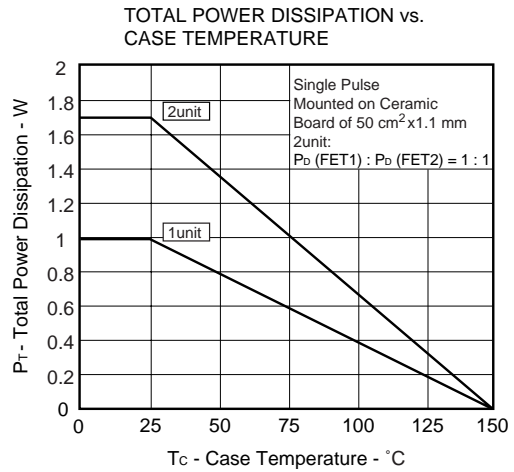
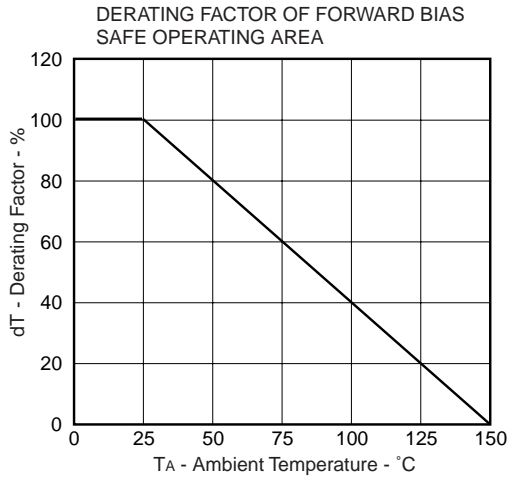
TEST CIRCUIT 2 SWITCHING TIME

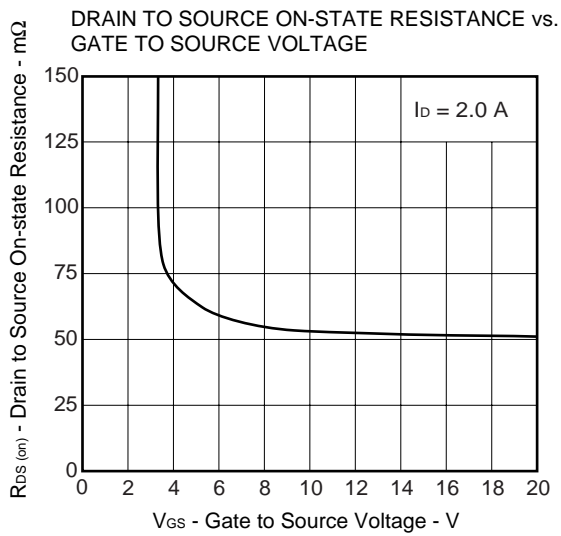
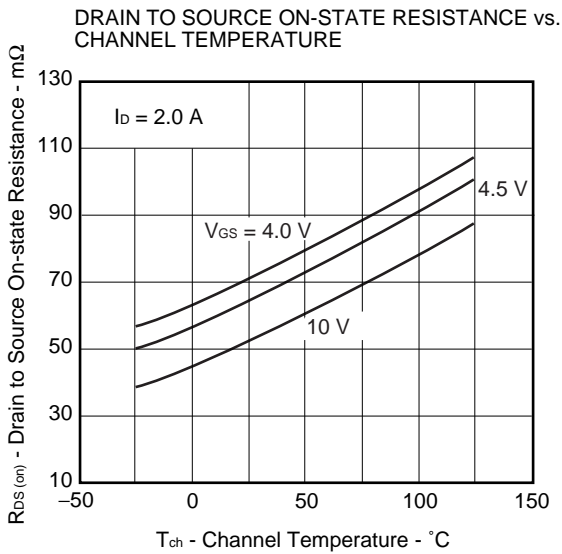
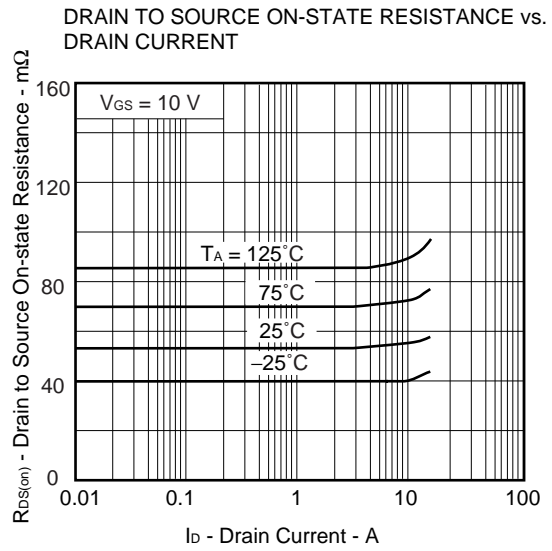
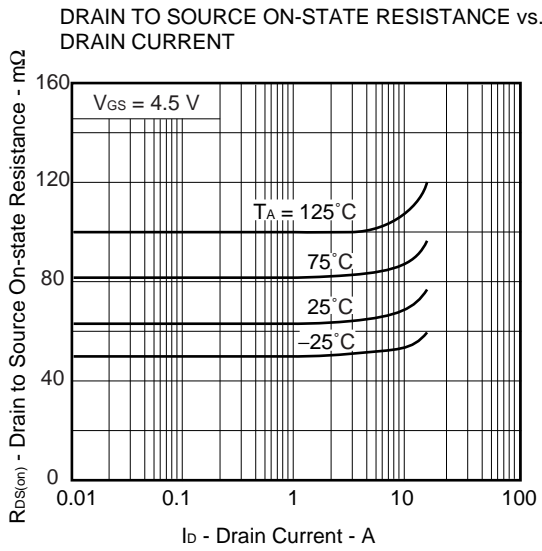
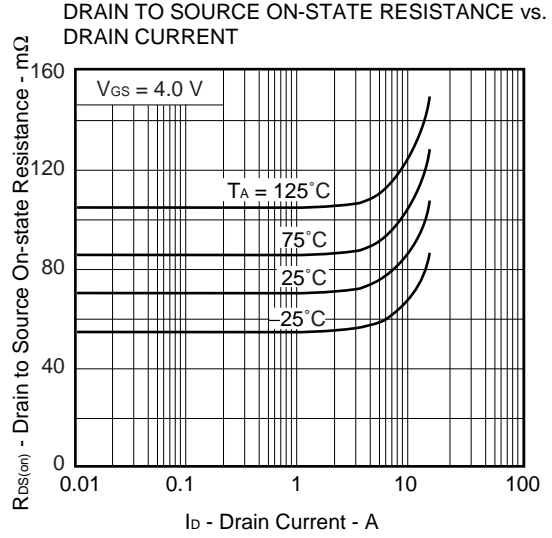
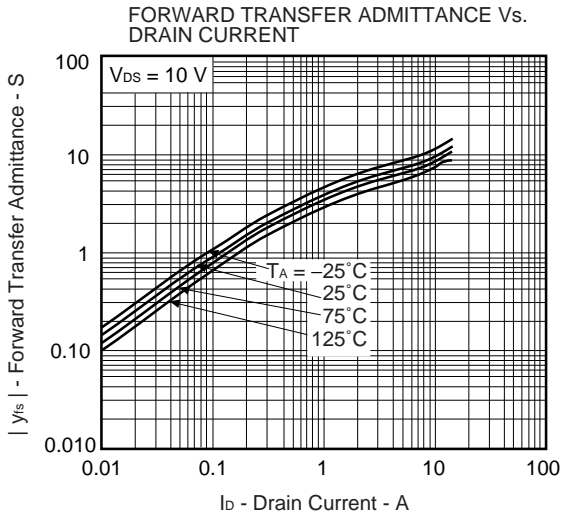


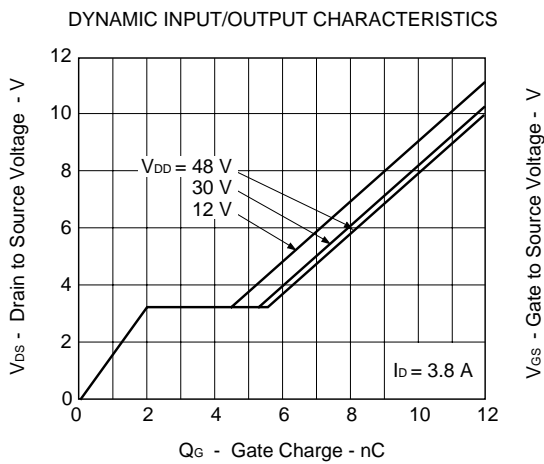
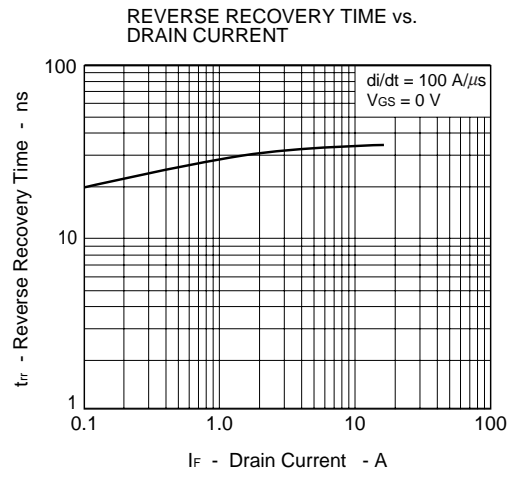
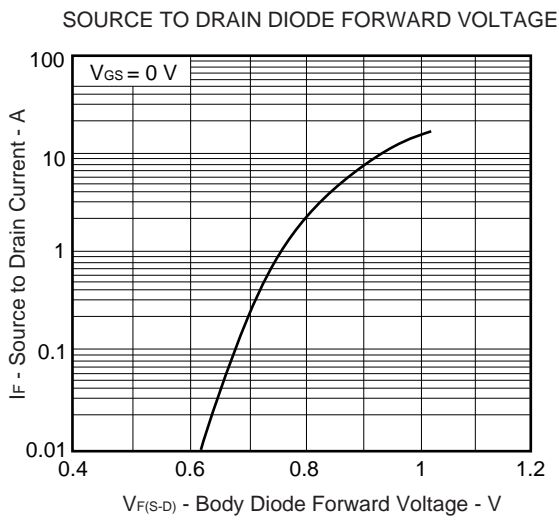
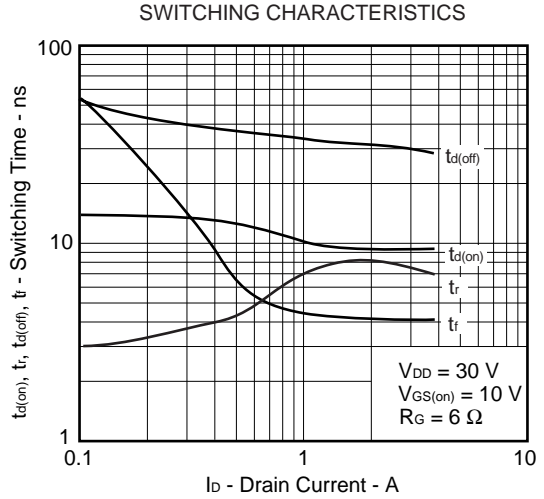
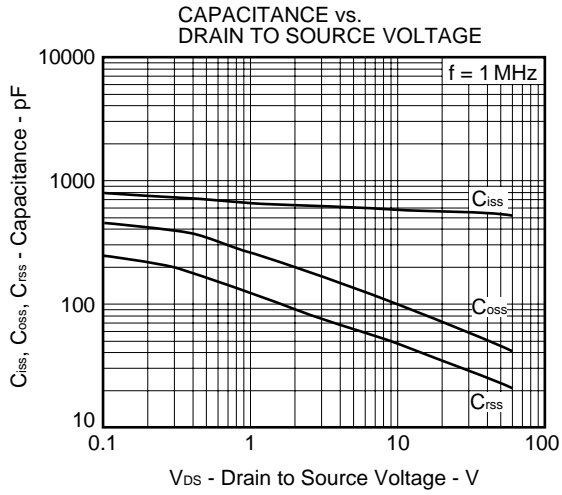
TEST CIRCUIT 3 GATE CHARGE

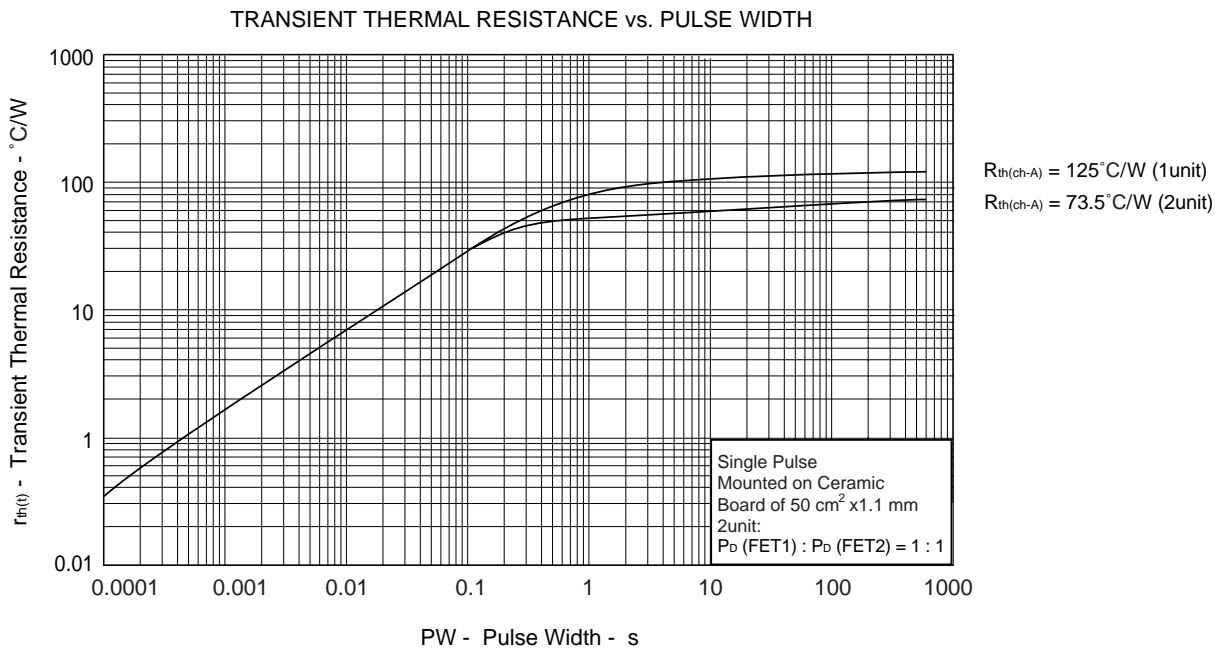
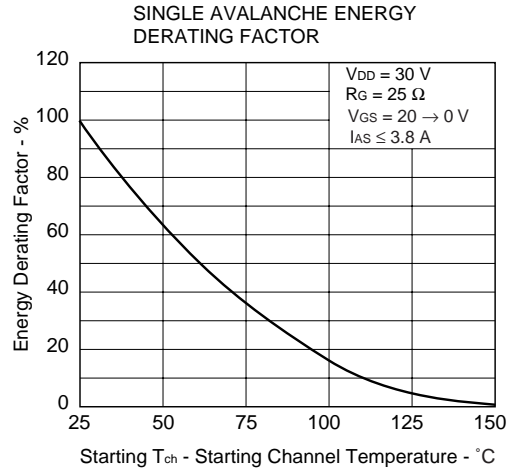
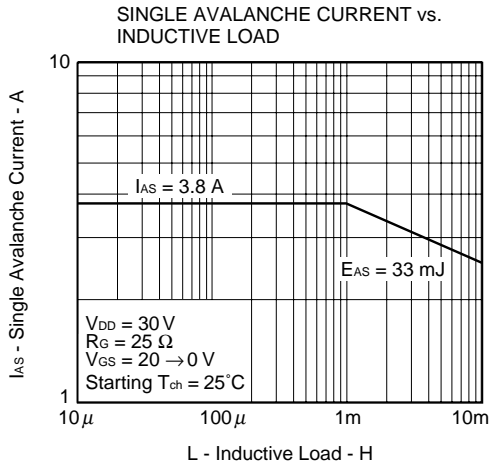


TYPICAL CHARACTERISTICS (T_A = 25°C)









[MEMO]

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